

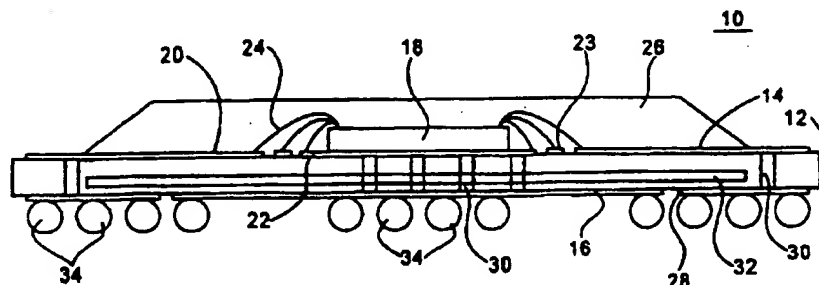
PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION  
International Bureau

## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

|  |  |  |   |
|--|--|--|---|
| (51) International Patent Classification <sup>6</sup> :<br>H05K 7/06, 7/02, H01L 23/48   |  | A1   | (11) International Publication Number:<br>WO 97/36466             |
|  |  |  | (43) International Publication Date:<br>2 October 1997 (02.10.97) |
| (21) International Application Number:<br>PCT/US97/03511   |  | (81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, GH, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). |   |
| (22) International Filing Date:<br>7 March 1997 (07.03.97)   |  |  |   |
| (30) Priority Data:<br>08/623,355      28 March 1996 (28.03.96)      US  |  |  |   |
| (71) Applicant (for all designated States except US): INTEL CORPORATION (US/US); 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). |  |  |   |
| (72) Inventor; and<br>(75) Inventor/Applicant (for US only): BARROW, Michael (US/US); 5000 Beechwood Court, El Dorado Hills, CA 95762 (US).  |  |  |   |
| (74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).  |  | Published<br>With international search report.   |   |

(54) Title: PERIMETER MATRIX BALL GRID ARRAY CIRCUIT PACKAGE WITH A POPULATED CENTER



## (57) Abstract

A ball grid array (BGA) integrated circuit package (10) which has an outer two-dimensional array of solder balls and a center two-dimensional array of solder balls (34) located on a bottom surface (16) of a package substrate (12). The solder balls are typically reflowed to mount the package to a printed circuit board. Mounted to an opposite surface of the substrate is an integrated circuit (18) that is electrically coupled to the solder balls by internal routing within the package. The outer array of solder balls are located outside of the dimensional profile of the integrated circuit to reduce solder stresses induced by the differential thermal expansion between the integrated circuit and the substrate. The center solder balls are typically routed directly to ground and power pads of the package to provide a direct thermal and electrical path from the integrated circuit to the printed circuit board.

BRCM 832708

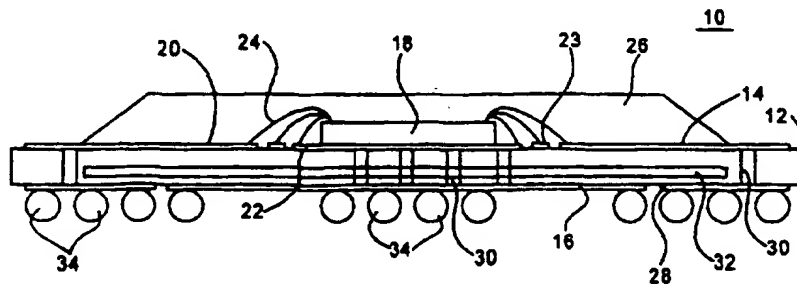
PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION  
International Bureau

## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

|  |  |  |   |
|--|--|--|---|
| (51) International Patent Classification <sup>6</sup> :<br><b>H05K 7/06, 7/02, H01L 23/48</b>  |  | A1   | (11) International Publication Number:<br><b>WO 97/36466</b>      |
|  |  |  | (43) International Publication Date:<br>2 October 1997 (02.10.97) |
| (21) International Application Number:<br><b>PCT/US97/03511</b>  |  | (81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, GH, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). |   |
| (22) International Filing Date:<br><b>7 March 1997 (07.03.97)</b>  |  | Published<br>With international search report.   |   |
| (30) Priority Data:<br><b>08/623,355 28 March 1996 (28.03.96) US</b>   |  |  |   |
| (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). |  |  |   |
| (72) Inventor; and<br>(75) Inventor/Applicant (for US only): BARROW, Michael [US/US]; 5000 Beechwood Court, El Dorado Hills, CA 95762 (US).  |  |  |   |
| (74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).  |  |  |   |

(54) Title: PERIMETER MATRIX BALL GRID ARRAY CIRCUIT PACKAGE WITH A POPULATED CENTER



## (57) Abstract

A ball grid array (BGA) integrated circuit package (10) which has an outer two-dimensional array of solder balls and a center two-dimensional array of solder balls (34) located on a bottom surface (16) of a package substrate (12). The solder balls are typically reflowed to mount the package to a printed circuit board. Mounted to an opposite surface of the substrate is an integrated circuit (18) that is electrically coupled to the solder balls by internal routing within the package. The outer array of solder balls are located outside of the dimensional profile of the integrated circuit to reduce solder stresses induced by the differential thermal expansion between the integrated circuit and the substrate. The center solder balls are typically routed directly to ground and power pads of the package to provide a direct thermal and electrical path from the integrated circuit to the printed circuit board.

BRCM 832709

**FOR THE PURPOSES OF INFORMATION ONLY**

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

|    |                          |    |  |    |  |    |                          |
|----|--------------------------|----|--|----|--|----|--------------------------|
| AL | Albania                  | ES | Spain                                    | LS | Lesotho                                      | SI | Slovenia                 |
| AM | Armenia                  | FI | Finland                                  | LT | Lithuania                                    | SK | Slovakia                 |
| AT | Austria                  | FR | France                                   | LU | Luxembourg                                   | SN | Senegal                  |
| AU | Australia                | GA | Gabon                                    | LV | Latvia                                       | SZ | Switzerland              |
| AZ | Azerbaijan               | GB | United Kingdom                           | MC | Monaco                                       | TD | Chad                     |
| BA | Bosnia and Herzegovina   | GE | Georgia                                  | MD | Republic of Moldova                          | TG | Togo                     |
| BB | Barbados                 | GH | Ghana                                    | MG | Madagascar                                   | TJ | Tajikistan               |
| BE | Belgium                  | GN | Guinea                                   | MK | The former Yugoslav<br>Republic of Macedonia | TM | Turkmenistan             |
| BF | Burkina Faso             | GR | Greece                                   | ML | Mali   | TR | Turkey                   |
| BG | Bulgaria                 | HU | Hungary                                  | MN | Mongolia                                     | TT | Trinidad and Tobago      |
| BJ | Benin                    | IE | Ireland                                  | MR | Mauritania                                   | UA | Ukraine                  |
| BR | Brazil                   | IL | Israel                                   | MW | Malawi                                       | UG | Uganda                   |
| BY | Belarus                  | IT | Italy                                    | MX | Mexico                                       | US | United States of America |
| CA | Canada                   | JP | Japan                                    | NE | Niger  | UZ | Uzbekistan               |
| CF | Central African Republic | KE | Kenya                                    | NL | Netherlands                                  | VN | Viet Nam                 |
| CG | Congo                    | KG | Kyrgyzstan                               | NO | Norway                                       | YU | Yugoslavia               |
| CH | Switzerland              | KP | Democratic People's<br>Republic of Korea | NZ | New Zealand                                  | ZW | Zimbabwe                 |
| CI | Côte d'Ivoire            | KR | Republic of Korea                        | PL | Poland                                       |    |                          |
| CM | Cameroon                 | KZ | Kazakhstan                               | PT | Portugal                                     |    |                          |
| CN | China                    | LC | Saint Lucia                              | RO | Romania                                      |    |                          |
| CU | Cuba                     | LJ | Liechtenstein                            | RU | Russian Federation                           |    |                          |
| CZ | Czech Republic           | LK | Sri Lanka                                | SD | Sudan  |    |                          |
| DE | Germany                  | LR | Liberia                                  | SE | Sweden                                       |    |                          |
| DK | Denmark                  |    |  | SG | Singapore                                    |    |                          |
| EE | Estonia                  |    |  |    |  |    |                          |

BRCM 832710

PERIMETER MATRIX BALL GRID ARRAY CIRCUIT  
PACKAGE WITH A POPULATED CENTER

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to an integrated circuit package.

2. DESCRIPTION OF RELATED ART

Integrated circuits are typically mounted to a package that is soldered to a printed circuit board. One such type of integrated circuit package is a ball grid array ("BGA") package. BGA packages have a plurality of solder balls located on a bottom external surface of a package substrate. The solder balls are reflowed to attach the package to the printed circuit board. The integrated circuit is mounted to a top surface of the package substrate, and electrically coupled to the solder balls by internal routing within the package.

Figure 1 shows a solder ball array of a prior art BGA package 2. The solder balls 4 are arranged in a two-dimensional pattern across the bottom surface of the package. The integrated circuit 6 is centrally located on the opposite side of the package 2. The package 2 is typically constructed from a material which has a coefficient of thermal expansion that is different than the thermal expansion coefficient of the integrated circuit. It has been found that the differential thermal expansion between the integrated circuit and the package will induce temperature related stresses that fail solder joints in an area which corresponds to the outer edges of the circuit die.

BRCM 832711

Figure 2 shows a BGA package 2 of the prior art which has an outer two dimensional array of solder balls 4. The solder balls 4 are located away from the package area that is beneath the integrated circuit 6. Locating the solder balls 4 away from the integrated circuit 6 reduces the thermal stresses on the solder joints created by the differential expansion between the package and the integrated circuit. Although effective in reducing solder failure the outer array pattern limits the input/output (I/O) of the package. Additionally, the integrated circuit generates heat which conducts through the solder balls and into the printed circuit board. Locating the solder balls at the outer perimeter of the package increases the thermal path through the package substrate. The longer path increases the thermal impedance of the package and the junction temperature of the integrated circuit. It longer product life, lower thermal impedance and higher I/O than BGA packages of the prior art.

#### SUMMARY OF THE INVENTION

The present invention is a ball grid array ("BGA") integrated circuit package which has an outer two-dimensional array of solder balls and a center two-dimensional array of solder balls located on a bottom surface of a package substrate. The solder balls are typically reflowed to mount the package to a printed circuit board. Mounted to an opposite surface of the substrate is an integrated circuit that is electrically coupled to the solder balls by internal routing within the package. The outer array of solder balls are located outside the dimensional profile of the integrated circuit to reduce solder stresses induced by the differential thermal expansion between the

integrated circuit and the substrate. The center solder balls are typically routed directly to ground and power pads of the package to provide a direct thermal and electrical path from the integrated circuit to the printed circuit board.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, wherein:

Figure 1 is a bottom view of a ball grid array integrated circuit package of the prior art;

Figure 2 is a bottom view of a ball grid array integrated circuit package of the prior art;

Figure 3 is a side cross-sectional view of a ball grid array package of the present invention;

Figure 4 is a bottom view of the package shown in Fig. 3;

Figure 5 is a bottom view of an alternate ball grid array package.

#### DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings more particularly by reference numbers, Figures 3 and 4 shows a ball grid array ("BGA") integrated circuit package 10 of the present invention. The package 10 includes a substrate 12 that has a top surface 14 and an opposite bottom surface 16. Mounted to the top surface 14 of the substrate 12 is an integrated circuit 16. The integrated circuit 18 is typically a microprocessor. Although a microprocessor is described, it is to be understood that the package 10 may contain any electrical device(s).

The top surface 14 of the substrate 12 has a plurality of bond pads 20 and a ground bus 22. The substrate 12 may also have a separate power bus 23 concentrically located about the integrated circuit 18 and ground pad 22. The integrated circuit 18 is coupled to the bond pads 20 and busses 22 and 23 by bond wires 24. The integrated circuit 16 is typically enclosed by an encapsulant 26. Although bond wires 24 are shown and described, the integrated circuit 18 can be mounted and coupled to the substrate with solder balls located on the bottom surface of the circuit die in a package and process commonly referred to as "C4" or "flip chip" packaging.

The bottom surface 16 of the substrate 12 has a plurality of contact pads 28. The contact pads 28 are coupled to the bond pads 20 and busses 22 and 23 by vias 30 and internal routing 32 within the substrate 12. The substrate can be constructed with conventional printed circuit board, or co-fired ceramic, packaging processes known in the art.

A plurality of solder balls 34 are attached to the contact pads 28 with known ball grid array processes. The solder balls 34 are typically reflowed to attach the package 10 to a printed circuit board (not shown).

The contact pads 28 are arranged in an outer two-dimensional array 36 and a center two-dimensional array 38. Each array contains a plurality of contact pads 28 that are separated from each other by a number of dielectric spaces 40. The outer array 36 is separated from the center array 38 by a dielectric area 42. The outer array 38 is preferably located outside of the outer dimensional profile of the integrated circuit 18. In this manner the solder joints of the outer array 38 are not subjected to stresses created by the difference in the coefficient of thermal expansion of the integrated circuit 18 and the expansion coefficient of

the substrate 12. The center array 38 is located near the origin of the integrated circuit 16 in an area that does not undergo as much thermal expansion as the outer edges of the circuit die. Therefore the solder stresses created by the differential thermal expansion is minimal in the area of the center array 38. The separated arrays provide a pattern that minimizes the stresses on the solder joints.

The outer array 36 is typically coupled to the signal lines of the integrated circuit 16. The center array 38 is preferably coupled to the ground bus 20 and power bus 23 of the substrate 12. The vias 30 that couple the busses 22 and 23 to the center contact pads 38 provide a direct thermal path through the substrate. The direct path lowers the thermal impedance of the package 10 and the junction temperature of the integrated circuit 18. Additionally, the short electrical path lowers the self-inductance and reduces the switching noise of the integrated circuit 18.

In the preferred embodiment, the package 10 contains 292 contact pads 28 on a 27 by 27 millimeter (mm) wide substrate 12, or 352 contact pads 28 on a 35 by 35 mm substrate 12. The dielectric space 40 between the contact pads 28 is typically 1.27 mm. The package 10 typically has a height of approximately 2.5 mm.

The package 10 is assembled by attaching the solder balls 34 to the contact pads 28. The integrated circuit 18 is mounted and coupled to the substrate 12. The integrated circuit 18 is then enclosed by the encapsulant 26. The BGA package 10 is typically shipped to an end user that mounts the package 10 to a printed circuit board by reflowing the solder balls 34.

Figure 5 shows an alternate embodiment of a package 10' which has five or six rows of contact pads 28 in the outer array 36' of the substrate 12'. The additional pads 28 increase the input/output (I/O) of the package



10. The outer array 36' is preferably outside the outer dimensional profile of the integrated circuit 18 to minimize the stresses on the solder joints. The package 10' may provide 324 contact pads 28 on a 27 by 27 mm substrate 10. The longer rows of the package 60 provide the approximate I/O of a 35 by 35 mm package, within the footprint of a 27 by 27 mm package.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art.

## CLAIMS

What is claimed is:

1. A ball grid array package, comprising:  
a substrate which has a top surface and an opposite bottom surface, said bottom surface having an outer array of contact pads each separated from each other by a first distance, and a center array of contact pads each separated from each other by a second distance, said center array of contact pads being separated from said outer array of contact pads by a third distance which is larger than the first and second distances; and,  
a plurality of solder balls attached to said contact pads of said substrate.
2. The package as recited in claim 1, wherein said top surface of said substrate has a plurality of bond pads.
3. The package as recited in claim 2, wherein said top surface of said substrate has a ground bus that is connected to said center array of contact pads by a plurality of vias that extend through said substrate.
4. The package as recited in claim 3, wherein said outer array of contact pads has at least five rows of contact pads.
5. The package as recited in claim 4, wherein said top surface of said substrate has a power bus that is connected to said center array of contact pads by a plurality of vias that extend through said substrate.

6. The package as recited in claim 5, wherein said center array of contact pads is arranged in a four by four matrix.

7. A ball grid array integrated circuit package, comprising:

a substrate which has a top surface and an opposite bottom surface, said top surface having a plurality of bond pads, said bottom surface having an outer array of contact pads each separated from each other by a first distance, and a center array of contact pads each separated from each other by a second distance, said center array of contact pads being separated from said outer array of contact pads by a third distance which is larger than the first and second distances;

a plurality of solder balls attached to said contact pads of said substrate; and,

an integrated circuit that is mounted to said substrate and coupled to said bond pads.

8. The package as recited in claim 7, wherein said top surface of said substrate has a ground bus that is coupled to said integrated circuit and connected to said center array of contact pads by a plurality of vias that extend through said substrate.

9. The package as recited in claim 8, wherein said outer array of contact pads has at least five rows of contact pads.

10. The package as recited in claim 9, wherein said top surface of said substrate has a power bus that is connected to said center array of contact pads by a plurality of vias that extend through said substrate.

11. The package as recited in claim 10, wherein said center array of contact pads is arranged in a four by four matrix.

12. The package as recited in claim 11, wherein said integrated circuit is enclosed by an encapsulant.

13. The package as recited in claim 7, wherein said outer array of contact pads is located outside an outer dimensional profile of said integrated circuit.

14. A method for assembling a ball grid array integrated circuit package, comprising the steps of:

a) providing a substrate which has a top surface and an opposite bottom surface, said bottom surface having an outer array of contact pads each separated from each other by a first distance, and a center array of contact pads each separated from each other by a second distance, said center array of contact pads being separated from said outer array of contact pads by a third distance which is larger than the first and second distances;

b) mounting an integrated circuit to said top surface of said substrate; and,

c) attaching a plurality of said solder balls to said contact pads.

15. The method as recited in claim 14, further comprising the step of encapsulating said integrated circuit.

16. The method as recited in claim 15, further comprising the step of coupling said integrated circuit to said substrate with a plurality of bond wires.

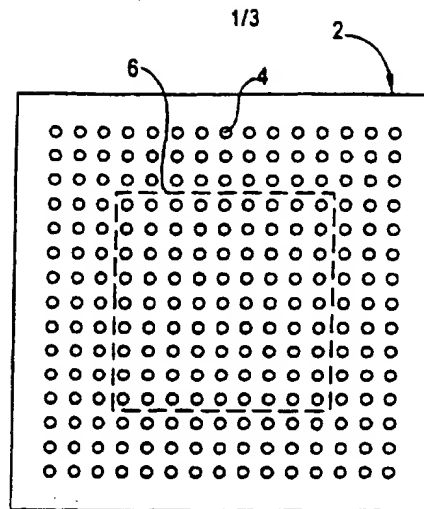


FIG. 1 PRIOR ART

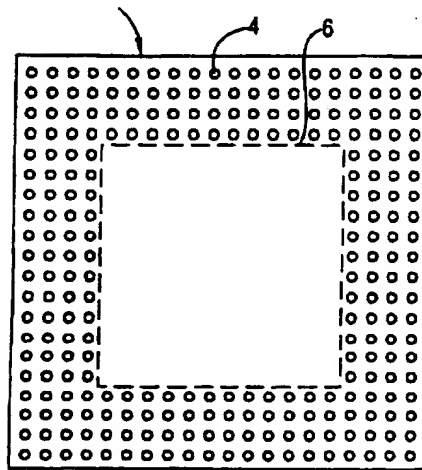
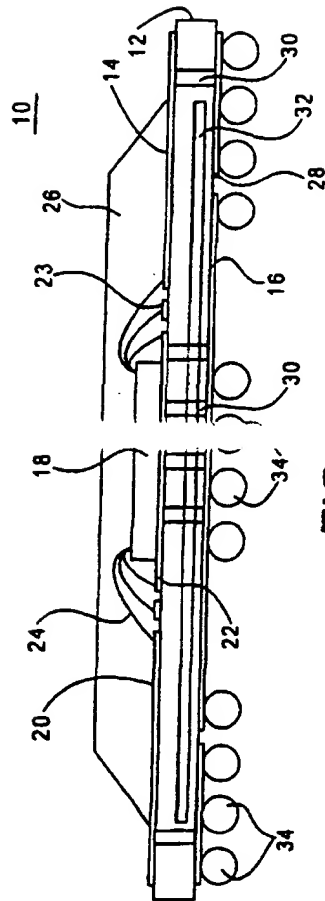


FIG. 2 PRIOR ART

SUBSTITUTE SHEET (RULE 26)

BRCM 832720



**FIG. 3**

**SUBSTITUTE SHEET (RULE 26)**

**BRCM 832721**

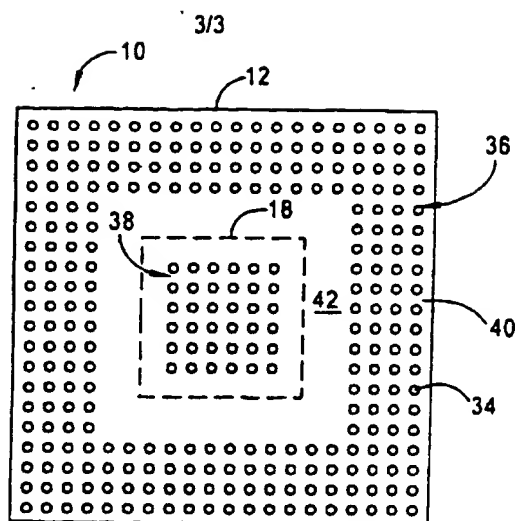


FIG. 4

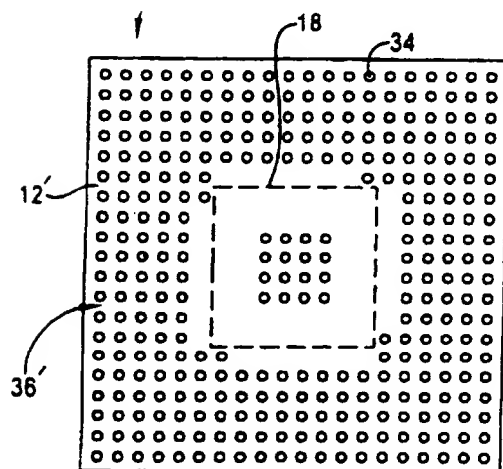


FIG. 5

SUBSTITUTE SHEET (RULE 26)

BRCM 832722

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US97/03511

|   |   |   |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
|---|---|---|--|-----|--|---|-----|--|---|-----|---|--|-----|--|---|--|--|---|--|--|
| <b>A. CLASSIFICATION OF SUBJECT MATTER</b><br>IPC(6) : H05K 7/06, 7/02; H01L 23/48<br>US CL : 361/760, 719; 257/787<br>According to International Patent Classification (IPC) or to both national classification and IPC  |   |   |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| <b>B. FIELDS SEARCHED</b><br>Minimum documentation searched (classification system followed by classification symbols)<br>U.S. : 361/760, 719, 704, 707, 720, 221; 257/787, 700, 747, 778, 723, 724<br>Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched<br>NONE.<br>Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)<br>NONE.  |   |   |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| <b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>   |   |   |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| Category*   | Citation of document, with indication, where appropriate, of the relevant passages                      | Relevant to claim No.   |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| X<br>---<br>Y   | US 5,490,324 A (NEWMAN) 13 February 1996, col. 8, lines 30-42, col. 11, lines 5-23 and Figures 4 and 5. | 1, 2, 6, 9, 12-16<br>---<br>3-5, 7, 8, 10, 11   |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
|   | lines 36-52 and Figure 2.   | 11  |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| Y   | US 5,450,283 A (LIN et al) 12 September 1995, see the entire document.                                  | 3-5, 7, 8, 10, 11   |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| A   | US 5,216,278 A (LIN et al) 01 June 1993, see the entire document.                                       | 1-16  |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| A   | US 5,285,352 A (PASTORE et al) 08 February 1994, see the entire document.                               | 1-16  |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| <input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.   |   |   |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| <table border="0"><tr><td>* Special categories of cited documents:</td><td>"T"</td><td>later documents published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</td></tr><tr><td>"A" documents defining the general state of the art which is not considered to be of particular relevance</td><td>"X"</td><td>document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</td></tr><tr><td>"E" earlier documents published on or after the international filing date</td><td>"Y"</td><td>document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combinations being obvious to a person skilled in the art</td></tr><tr><td>"L" documents which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</td><td>"A"</td><td>documents member of the same patent family</td></tr><tr><td>"O" documents referring to an oral disclosure, use, exhibition or other means</td><td></td><td></td></tr><tr><td>"P" documents published prior to the international filing date but later than the priority date claimed</td><td></td><td></td></tr></table> |   |   | * Special categories of cited documents: | "T" | later documents published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention | "A" documents defining the general state of the art which is not considered to be of particular relevance | "X" | document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone | "E" earlier documents published on or after the international filing date | "Y" | document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combinations being obvious to a person skilled in the art | "L" documents which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) | "A" | documents member of the same patent family | "O" documents referring to an oral disclosure, use, exhibition or other means |  |  | "P" documents published prior to the international filing date but later than the priority date claimed |  |  |
| * Special categories of cited documents:  | "T"   | later documents published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention  |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| "A" documents defining the general state of the art which is not considered to be of particular relevance   | "X"   | document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone  |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| "E" earlier documents published on or after the international filing date   | "Y"   | document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combinations being obvious to a person skilled in the art |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| "L" documents which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)  | "A"   | documents member of the same patent family  |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| "O" documents referring to an oral disclosure, use, exhibition or other means   |   |   |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| "P" documents published prior to the international filing date but later than the priority date claimed   |   |   |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| Date of the actual completion of the international search<br>23 APRIL 1997  |   | Date of mailing of the international search report<br>26 JUN 1997   |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |
| Name and mailing address of the ISA/US<br>Commissioner of Patents and Trademarks<br>Box PCT<br>Washington, D.C. 20231<br>Facsimile No. (703) 305-3230   |   | Authorized officer<br>DAVID FOSTER<br>Telephone No. (703) 308-4760  |  |     |  |   |     |  |   |     |   |  |     |  |   |  |  |   |  |  |

Form PCT/ISA/210 (second sheet) (July 1992)

BRCM 832723